Chapter 2: Diode Applications

2.1 Half Wave Rectifiers:

The simplest of networks to examine with AC signal appears in Figure 2.1.

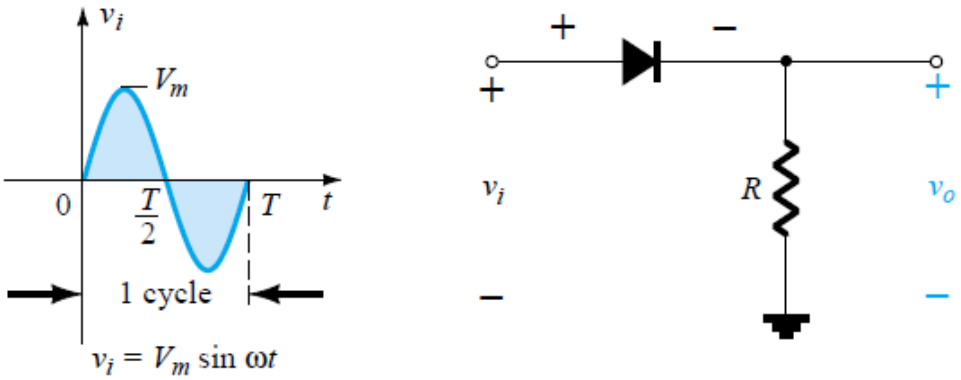


Figure 2.1: Half-wave rectifier.

a. During the interval $t = 0$ to $T/2$ in Figure 2.1, the polarity of the applied voltage *vi* is positive (as shown in the above figure), this Turns the Diode into ON-State (short Circuit) assuming Ideal diode. As shown in figure below, the output voltage is the same as the input voltage.

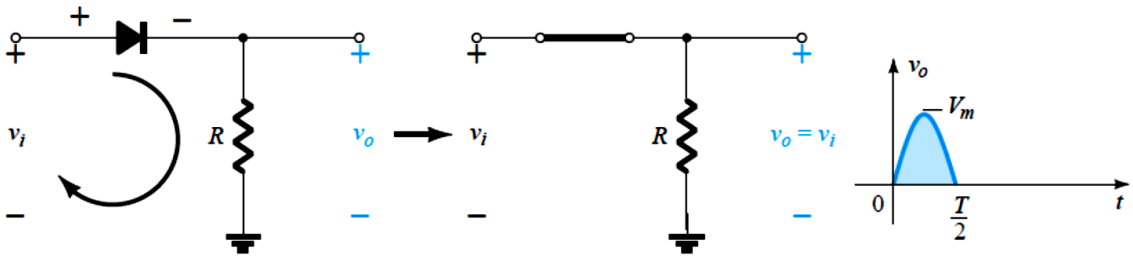


Figure 2.2: Conduction region (0 → T/2).

b. For the period $T/2 \rightarrow T$, : during this period the negative side of the input signal is applied to the diode which makes the diode OFF (open Circuit) and the output is Zero.

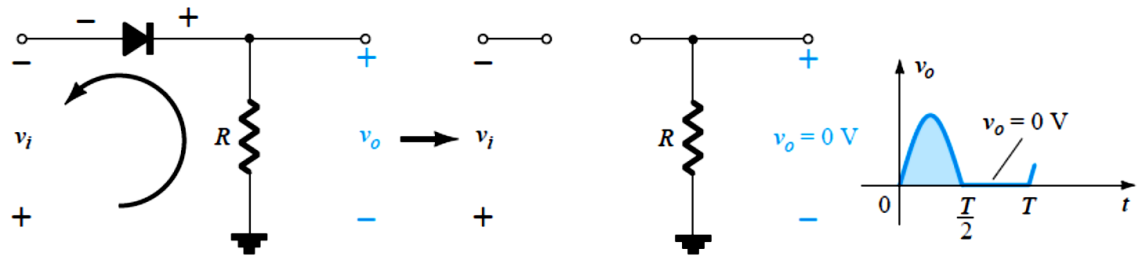


Figure 2.3: Non-conduction region (T/2 → T).

$$V_{dc} = \frac{1}{T}\int_0^T V_i\, dt$$

$$V_{dc} = \frac{1}{T}\int_0^T V_m \sin wt\, dt$$

$$V_{dc} = \frac{1}{T}\int_0^{\frac{T}{2}} V_m \sin wt\, dt$$

$$V_{dc} = \frac{V_m}{wT}[-\cos wt]_0^{T/2}$$

$$V_{dc} = \frac{V_m}{wT}\left[-\cos\frac{wT}{2} + \cos\ 0\right]_0^{T/2}, w = 2\pi f = \frac{2\pi}{T}$$

$$\boldsymbol{V_{dc} = 0.318\, V_m}$$

Root Mean Square Voltage (RMS Voltage):

$$V_{rms} = \sqrt{\frac{1}{T}\int_0^T {V_i}^2\, dt}$$

$$V_{rms} = \sqrt{\frac{1}{T}\int_0^T (V_m \sin wt)^2\, dt}$$

$$V_{rms} = \sqrt{\frac{1}{T}\int_0^{T/2} (V_m \sin wt)^2\, dt}$$

$$then, use: \sin^2 wt = \frac{1}{2}(1 - \cos 2wt)\ and\ w = 2\pi f = \frac{2\pi}{T}$$

$$V_{rms} = \frac{V_m}{2}$$

The process of removing one-half the input signal to establish a dc level is properly called *half-wave rectification.*

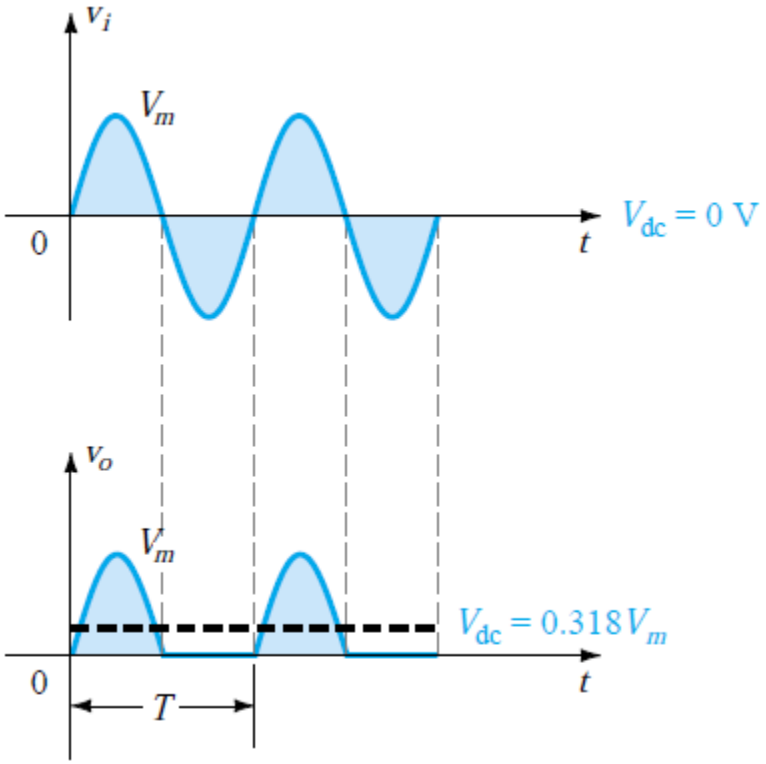


Figure 2.4: Half-wave rectified signal.

If the diode is practical the Vdc equation will be:

$$\boldsymbol{V_{dc} \cong 0.318(V_m - V_T)}$$

$$V_T = V_D = 0.7\ V\ for\ Si\ or\ 0.3\ for\ Ge - Diodes$$

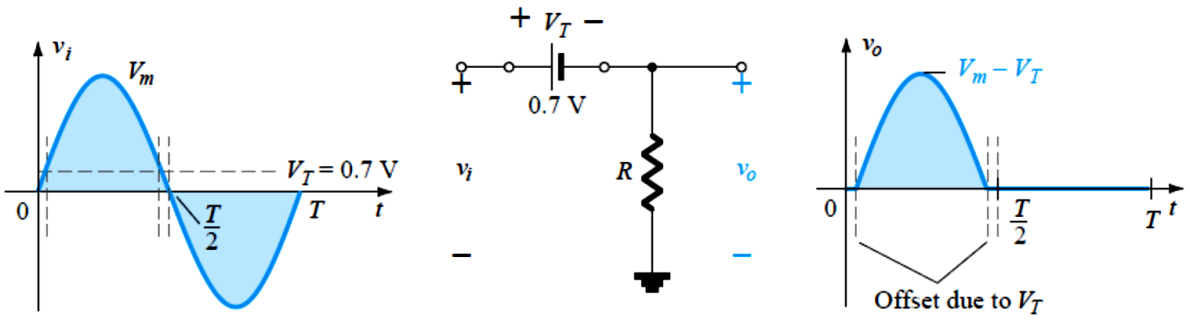


Figure 2.5: Effect of V_T on half-wave rectified signal.

Example: (a) Sketch the output *vo* and determine the dc level of the output for the circuit shown in Figure 2.6.

(b) Repeat part (a) if the ideal diode is replaced by a silicon diode.

(c) Repeat parts (a) and (b) if *Vm* is increased to 200 V and compare solutions using Ideal and silicon diodes.

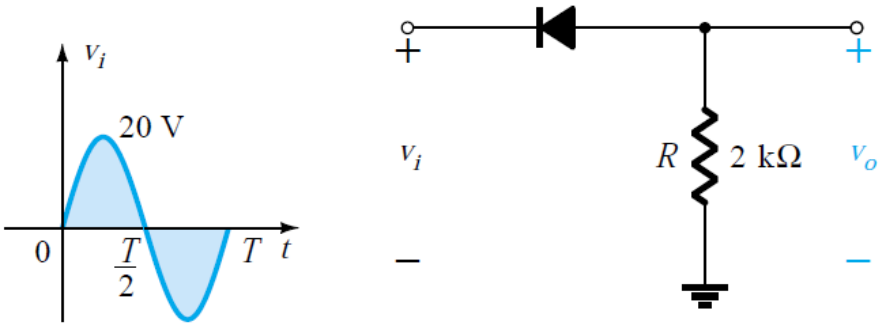


Figure 2.6: the circuit diagram.

a. In this situation the diode will conduct during the negative part of the input as shown in Fig. 2.7, and *vo* will appear as shown in the same figure. For the full period, the dc level is:

$$V_{dc} = -0.318Vm = -0.318(20\text{ V}) = \mathbf{-6.36\text{ V}}$$

The negative sign indicates that the polarity of the output is opposite to the defined polarity in Figure 2.6.

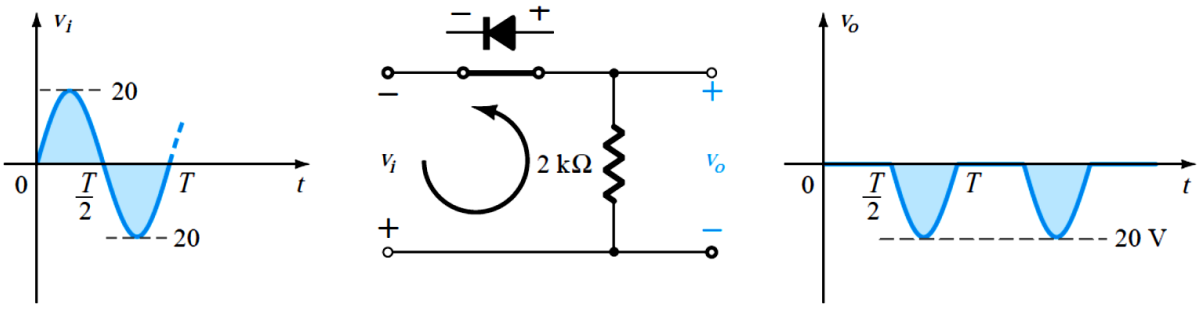


Figure 2.7: Resulting *vo* for the circuit of the example.

b. Using a silicon diode, the output has the appearance of Figure 2.8 and

$V_{dc} = -0.318(Vm - 0.7\text{ V}) = -0.318(19.3\text{ V}) = \mathbf{-6.14\text{ V}}$

The resulting drop in dc level is 0.22 V or about 3.5%.

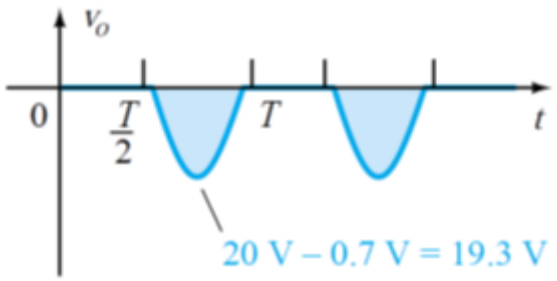


Figure 2.8: Effect of V_T on output.

c. Ideal diode: V_{dc}= - 0.318Vm= - 0.318(200 V) = - **63.6 V**

Silicon Diode: V_{dc}= - 0.318(Vm -VT)= - 0.318(200 V -0.7 V)= - (0.318)(199.3 V)

V_{dc} = - **63.38 V**

This small difference between the output voltage using ideal and silicon diodes can be ignored for most applications.

PIV (PRV)

The Peak Inverse Voltage (PIV) [or **PRV** (**Peak Reverse Voltage**)] rating of the diode is of primary importance in the design of rectification systems. Recall that it is the voltage rating that must not be exceeded in the reverse-bias region or the diode will enter the Zener avalanche region. The required PIV rating for the half-wave rectifier can be determined from Figure 2.9, which displays the reverse-biased diode of Figure 2.1with maximum applied voltage. Applying Kirchhoff's voltage law, it is fairly obvious that the PIV rating of the diode must equal or exceed the peak value of the applied voltage. Therefore,

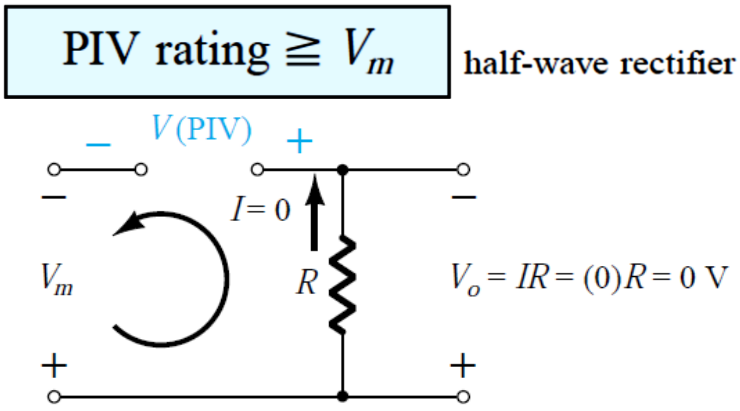


Figure 2.9: Determining the required PIV rating for the half wave rectifier.

2.2 Full Wave Rectifiers

The dc level obtained from a sinusoidal input can be improved 100% using a process called *full-wave rectification.*

2.2.1 *Bridge Rectifier*

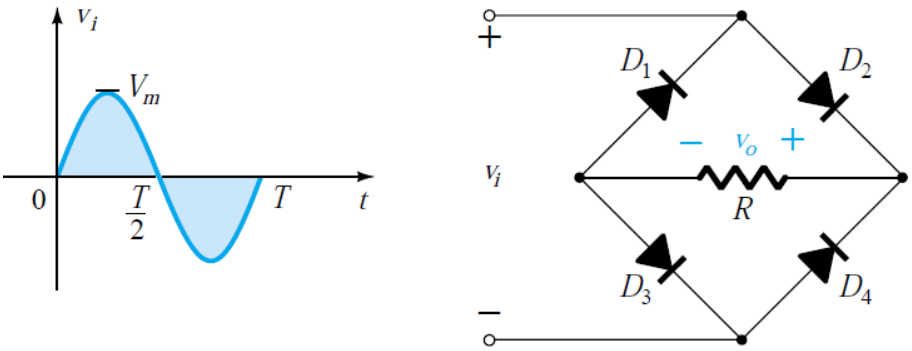


Figure 2.10: Full wave Bridge Rectifier.

During the Positive period:

- During the period t = 0 to $T/2$: D_2 and D_3 are conducting while D_1 and D_4 are in the "off" state.
- Since the diodes are ideal the load voltage is $v_o = v_i$, as shown in the Figure 2.12.

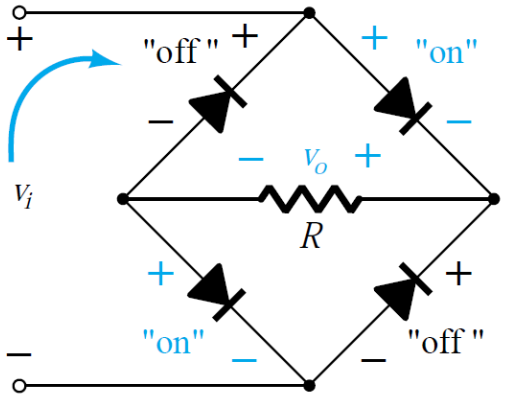


Figure 2.11: Full wave rectifier for the period 0 → T/2 of the input voltage vi.

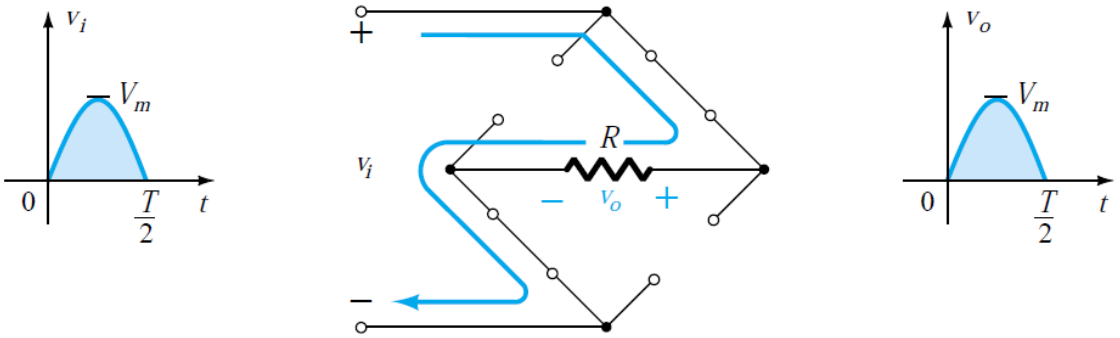


Figure 2.12: Conduction path for the positive region of vi.

During the Negative period:

- During the period t = 0 to $T/2$: D_1 and D_4 are conducting while D_2 and D_3 are in the "off" state.
- Since the diodes are ideal the load voltage is $v_o = v_i$, as shown in the Figure 2.13.

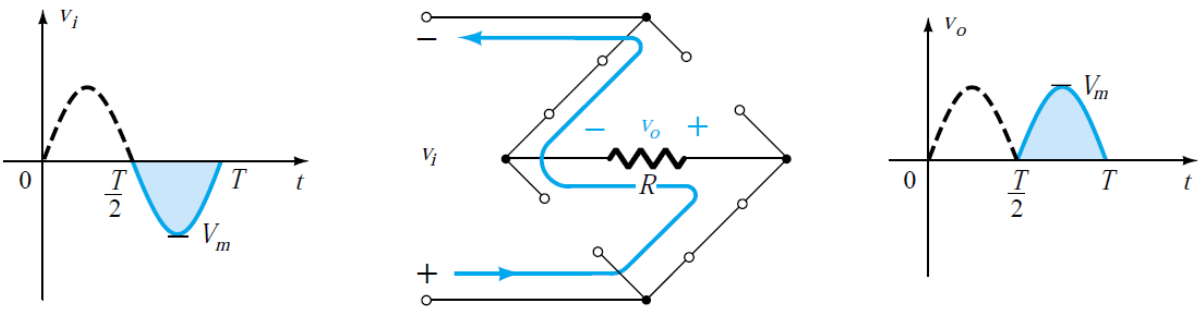


Figure 2.13: Conduction path for the negative region of vi.

- Over one full cycle the input and output voltages will appear as shown in Figure 2.14.

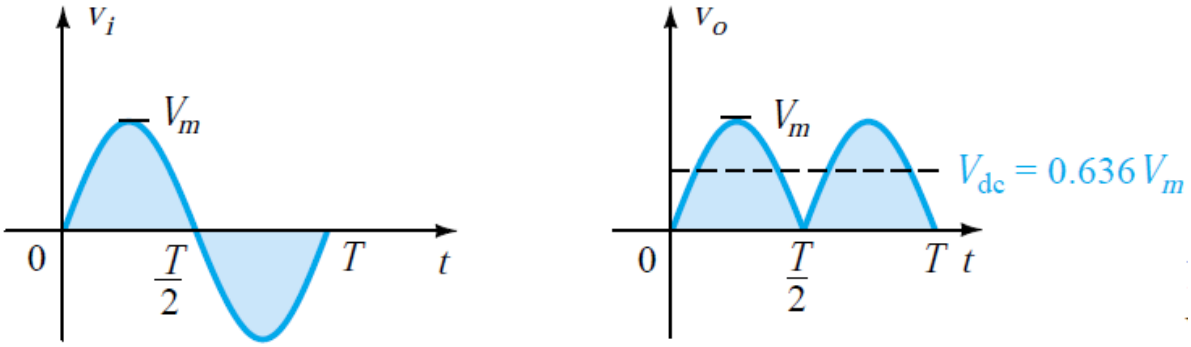


Figure 2.14: Input and output waveforms for a full-wave rectifier.

- For Ideal Diodes: The DC Voltage or Average Voltage: since the area above the axis for one full cycle is now twice that obtained for a half-wave system,

$$\boldsymbol{V_{dc} = 0.636\,V_m}$$

Prove it?

- For Practical Diodes (Si or Ge): The DC Voltage or Average Voltage:

$$\boldsymbol{V_{dc} \cong 0.636(V_m - 2V_T)}$$

This can be computed from Figure 2.15 as shown below:

KVL around the conduction path would result in

$$v_i - V_T - v_o - V_T = 0, \quad v_o = v_i - 2\,V_T$$

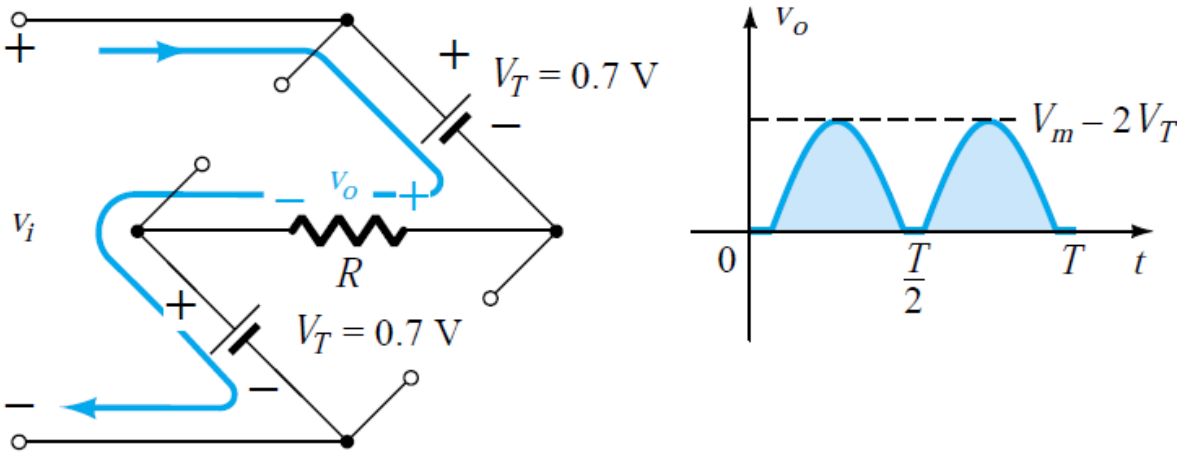


Figure 2.15: Determining Vo_{max} for practical diodes in the bridge configuration.

- The peak value of the output voltage v_o is therefore

$$V_{omax} = V_m - 2V_T$$

- Then the dc voltage:

$$V_{dc} \cong 0.636(V_m - 2V_T)$$

$$\boldsymbol{V_{rms} = 0.707\,V_m}$$

Prove it?

PIV

The required PIV of each diode (ideal) can be determined from Figure 2.16 obtained at the peak of the positive region of the input signal. For the indicated loop the maximum voltage across R is Vm and the PIV rating is defined by:

$\boldsymbol{PIV \geq V_m}$ **: Full-wave bridge rectifier.**

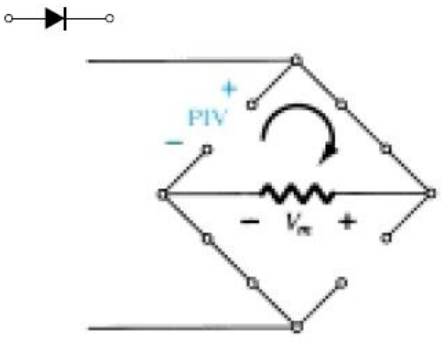


Figure 2.16: Determining the required PIV for the bridge configuration.

2.2.2 *Centre-Tapped Transformer*

A second popular full-wave rectifier appears in Figure 2.17 with only two diodes but requiring a centre-tapped (CT) transformer to establish the input signal across each section of the secondary of the transformer.

- During the positive portion of *vi* . *D*1 assumes the short-circuit equivalent and *D*2 the open-circuit equivalent. The output voltage appears as shown in Figure 2.18.
- During the Negative portion of *vi* . *D*2 assumes the short-circuit equivalent and *D*1 the open-circuit equivalent. The output voltage appears as shown in Figure 2.19.

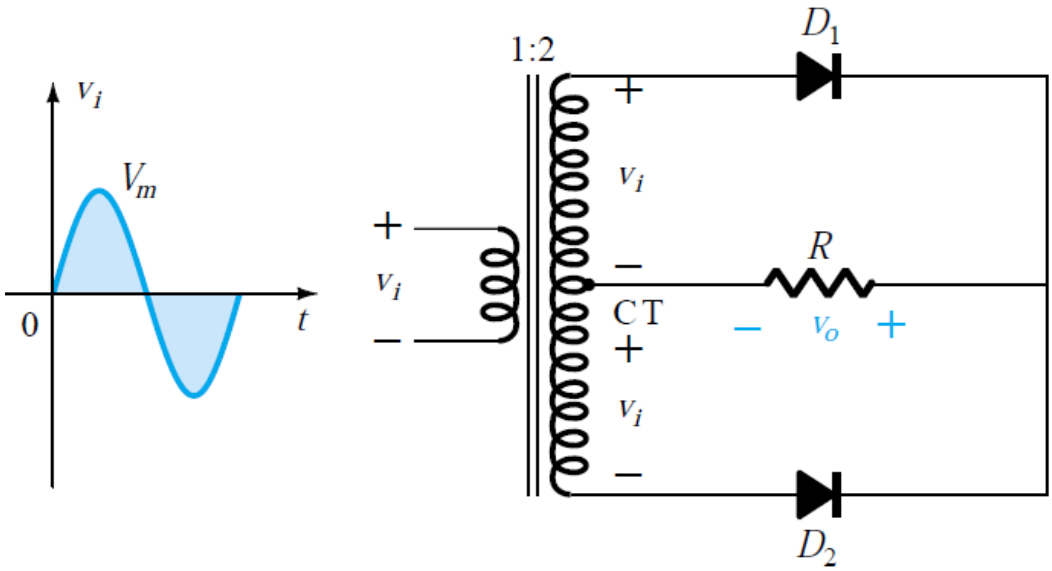


Figure 2.17: Centre-tapped transformer full-wave rectifier

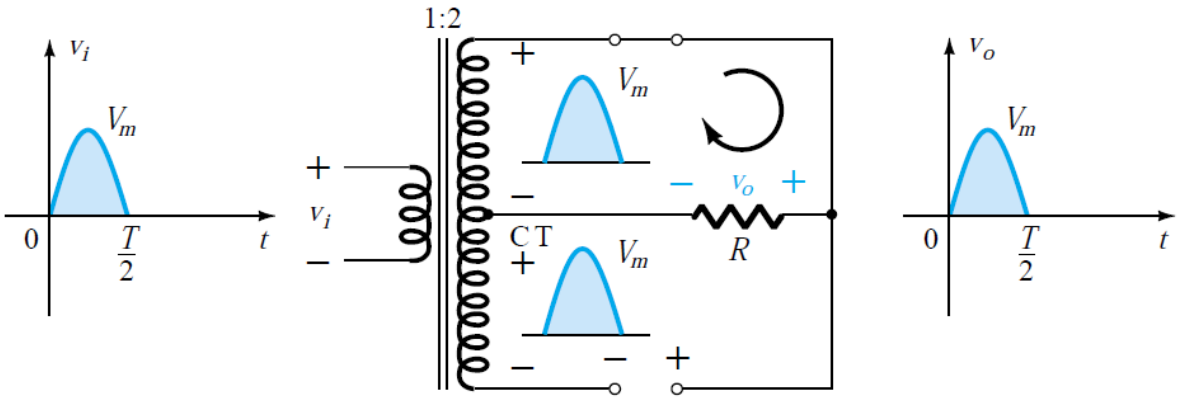


Figure 2.18: Network conditions for the positive region of vi.

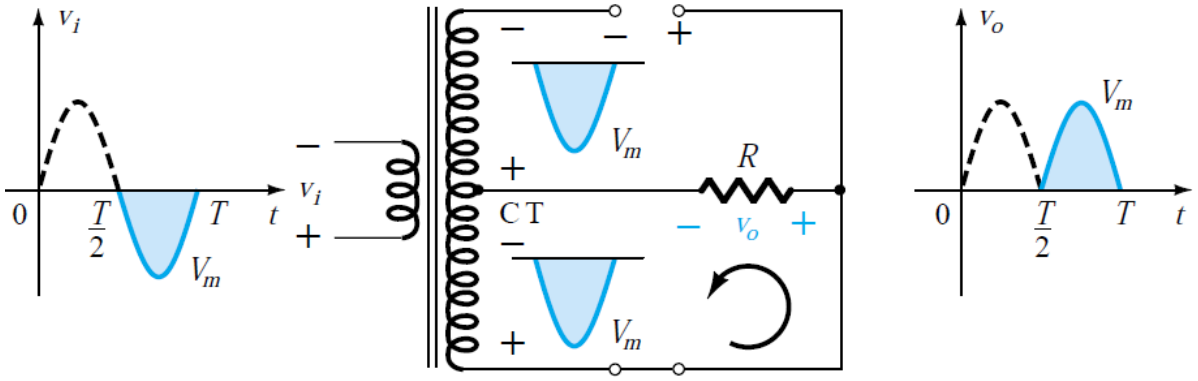


Figure 2.19: Network conditions for the negative region of v_i.

PIV

The network of Figure 2.20 will help us determine the net PIV for each diode for this full-wave rectifier. Inserting the maximum voltage for the secondary voltage and *Vm* as established by the adjoining loop will result in:

$$\text{PIV} = V_{\text{secondary}} + V_R$$
$$= V_m + V_m$$

$$\boxed{\text{PIV} \geq 2V_m}$$ CT transformer, full-wave rectifier

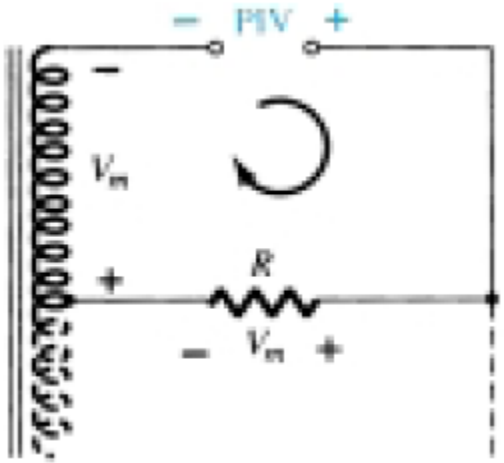
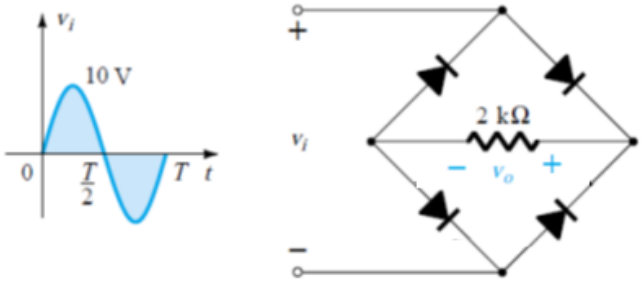


Figure 2.20: Determining the PIV level for the diodes of the CT transformer full-wave rectifier.

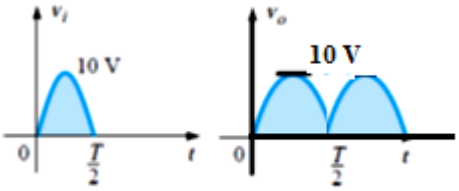
Example: Determine the output waveform for the circuit shown below and calculate the output dc level and the required PIV of each diode.



Vin can be written as vi= 10 Sin(wt), 10 means the maximum input voltage.

Solution:

The output waveform will be :



$$V_{dc} = 0.636(10\text{V}) = 6.36\ \mathbf{V}$$

The PIV is equal to the maximum voltage across *R*, which is **10 V**.

2.3 CLIPPERS

There are a variety of diode networks called *clippers* that have the ability to "clip" off a portion of the input signal without distorting the remaining part of the alternating waveform.

There are two general categories of clippers:

- *Series:* The diode is in series with the load. (HWR)
- *Parallel:* The diode in a branch parallel to the load.

2.3.1 Series

The response of the series clippers to a variety of alternating waveforms is provided in Figure 2.21-b.

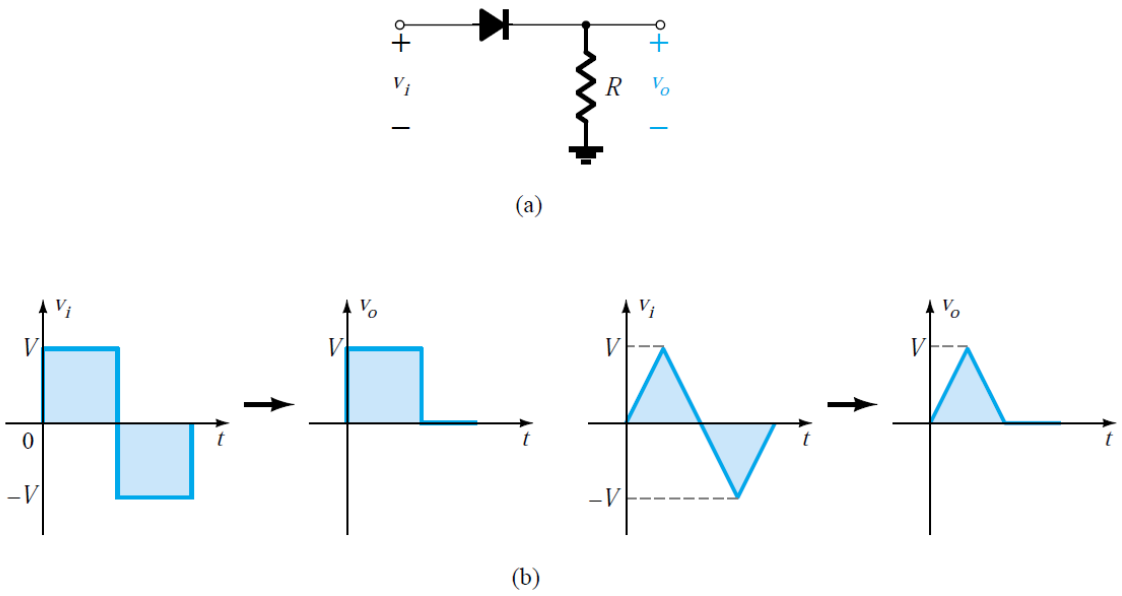


Figure 2.21: Series Clipper.

Example1: Determine the output waveform for the circuit of Figure 2.22.

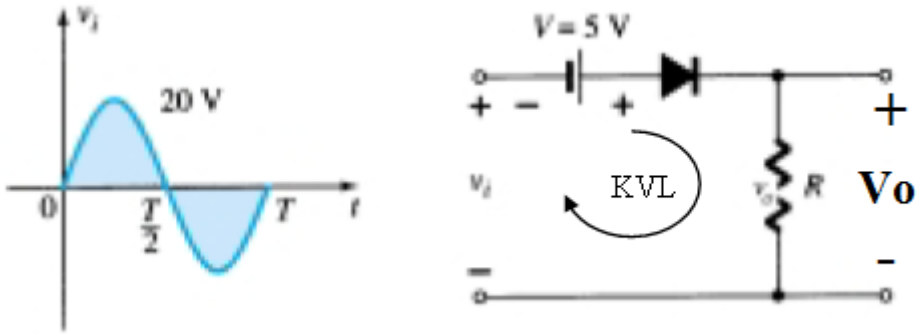


Figure 2.22: The circuit of Example1.

Note: Serial Clipper: ملاحظة عامة

- **If the Diode Off: Vo=Vx**

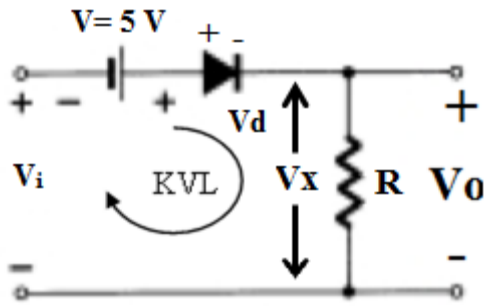
يعني الجمع الاتجاهي لمصادر الفولتية في فرع المقاومة (R) اذا كانت هناك مصادر للفولتية.

هنا في هذا المثال لا توجد مصادر فولتية لذلك : Vx=0

- **If the Diode ON: Vo= Apply KVL**

Solution:

During the positive part of the input signal:



KVL for the input loop of the above circuit:

+Vi +V –Vd –Vo = 0

The Diode is Ideal, thus Vd=0

Vi+5-Vo=0

Vo=Vi+5

This equation is valid when the diode is ON.

To Check the Diode state in the positive cycle:

Forward **(ON)**	**R**everse **(OFF)**
5 Volts	
Vi	

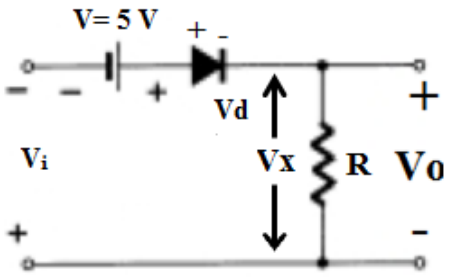
Therefore, the Diode is ON during the positive cycle. **The KVL equation MUST be Applied.**

هنا الدايود كان انحياز امامي لان جميع الفولتيات بالدائرة تجعلة منحاز اماميا

The results are tabulated in the following table:

Vi	**Vo=Vi+5**	Diode Status
0	5	ON
1	6	ON
2	7	ON
3	8	ON
4	9	ON
5	10	ON
6	11	ON
20	25	ON

During the Negative part of the input signal:



To Check the Diode state in the Negative cycle:

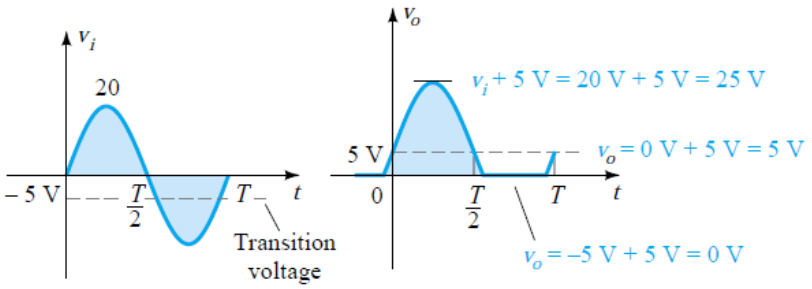
Forward (ON)	Reverse (OFF)
5 Volts	Vi

It means that the Diode is Forward (ON) if **Vi<5**

يعني ما دامت فولتية الادخال اقل من 5 فالديود يكون منحاز اماميا

يعني ان الفولتية في حالة ال 5 فولت تكون نقطة فاصلة بعدها يتحول الدايود الى منحاز عكسيا.

Vi	Vo	Diode Status	Notes
-1	4	ON	Vo=Vi+5نطبق معدلة كيرشهوف
-4	1	ON	Vo=Vi+5نطبق معدلة كيرشهوف
-5	**0**	**OFF**	**Vo=Vx; Vx=0**
-6	0	OFF	Vo=Vx; Vx=0
-20	0	OFF	Vo=Vx; Vx=0



Example2: Determine the output waveform for the circuit of Figure 2.23.

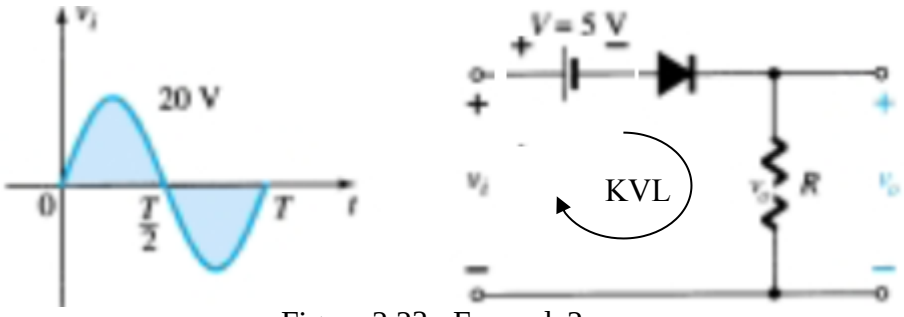


Figure 2.23: Example2.

Solution:

نطبق نفس الاجراءات في المثال السابق على هذه الدائرة

During the Positive Part, Apply KVL on the input loop:

+Vi – V –Vd –Vo=0

Vd=0, Diode Ideal

Vi -5-Vo=0

Vo=Vi-5

Forward **(ON)**	**R**everse **(OFF)**
Vi	5 Volts

Check the Diode status

The diode is **ON** when the input voltage **> 5** Volt, otherwise it is **OFF**.

Vi	Vo	Diode Status	Notes
0	0	OFF	Vo=Vx; Vx=0
1	0	OFF	Vo=Vx; Vx=0
2	0	OFF	Vo=Vx; Vx=0
3	0	OFF	Vo=Vx; Vx=0
4	0	OFF	Vo=Vx; Vx=0
5	**0**	**OFF**	**Vo=Vx; Vx=0**
6	1	ON	Vo=Vi-5نطبق معدلة كيرشهوف
20	15	ON	Vo=Vi-5نطبق معدلة كيرشهوف

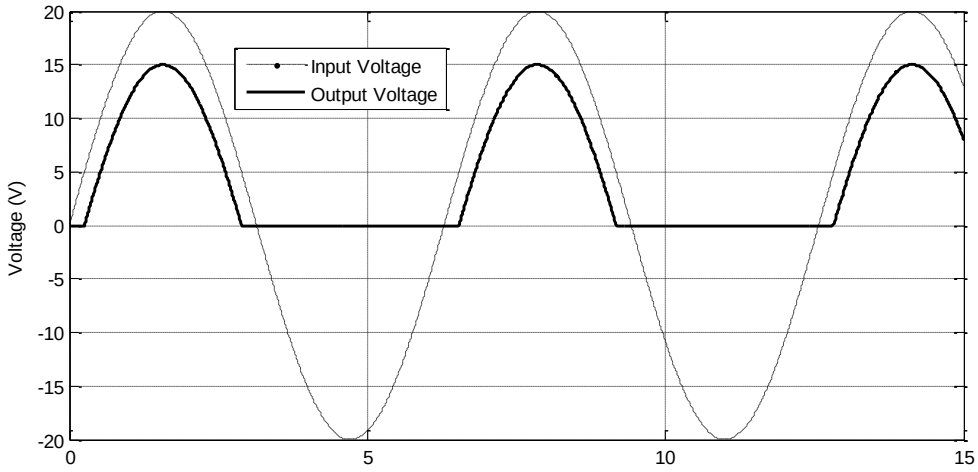
During the Negative Part, Apply KVL on the input loop:

Check the Diode status

Forward **(ON)**	**R**everse **(OFF)**
	5 Volts
	Vi

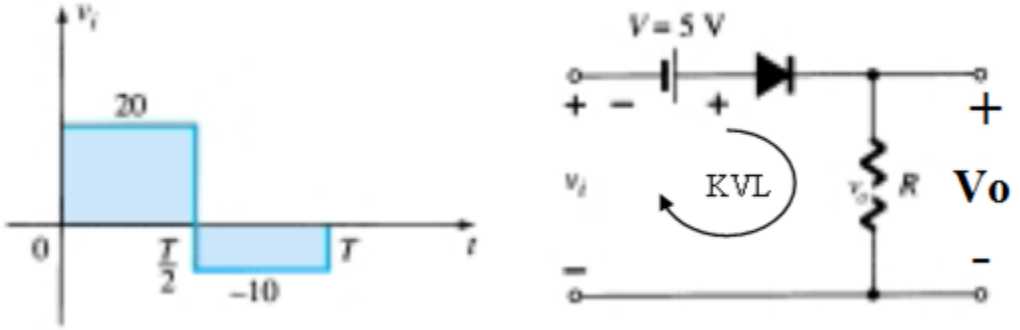
Therefore, the Diode is Always OFF and Vo=Vx

Vi	Vo	Diode Status	Notes
-1	0	OFF	Vo=Vx; Vx=0
-3	0	OFF	Vo=Vx; Vx=0
-4	0	OFF	Vo=Vx; Vx=0
-5	0	OFF	Vo=Vx; Vx=0
-6	0	OFF	Vo=Vx; Vx=0
-20	0	OFF	Vo=Vx; Vx=0



Output waveform of the Example2.

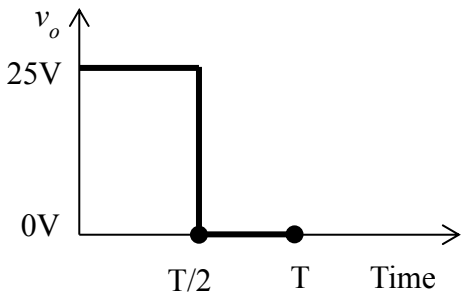
Example 3: Plot the output waveform of the following circuit.



Solution:

For *vi* = 20 V (0 → *T*/ 2) ; the diode is ON and *vo* =20 V + 5 V = 25 V.

For *vi*=-10 V; the diode is OFF and *vo* =0 V



H.W: Try the same examples by reversing the diode direction.

Parallel Clipper

The simplest of parallel diode configurations with the outputs are shown in Figure 2.24. The analysis of parallel configurations is very similar to that applied to series configurations, as demonstrated in the next examples.

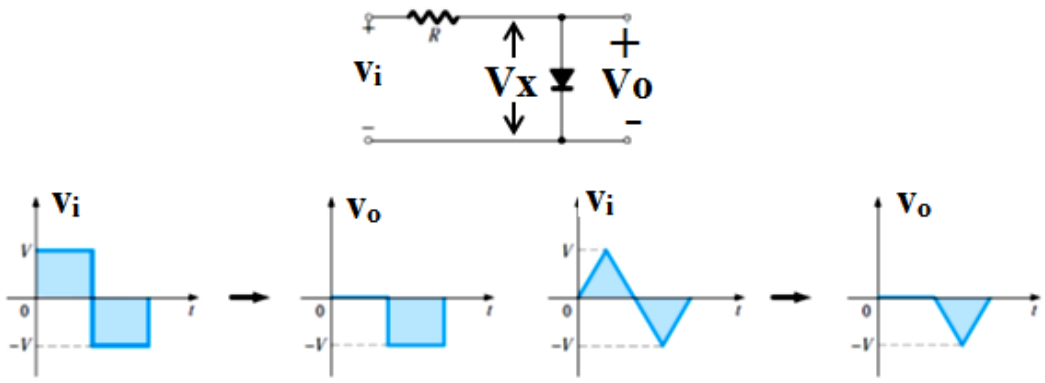


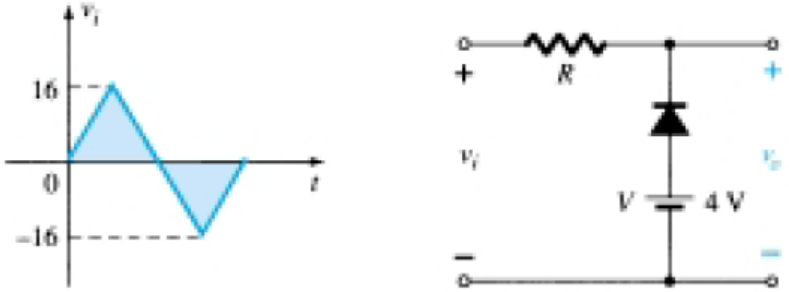
Figure 2.24: Response to a parallel clipper.

In parallel Clippers Remember the following rule:

Vo=Vx; if the diode ON

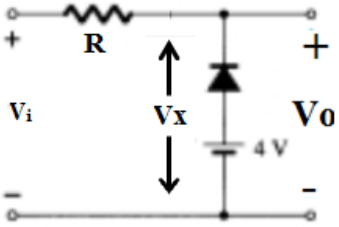
Vo=Vi; if the diode OFF

Example C: Determine v_o for the circuit shown in figure below:



Solution:

During the **Positive period**:



To Check the Diode state in the Positive cycle:

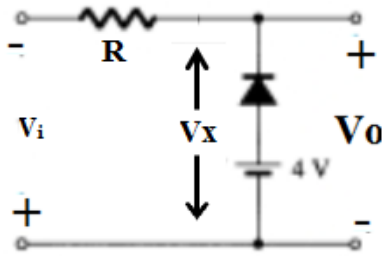
Forward (ON)	**Reverse (OFF)**
4 Volts	Vi

The diode is ON when the input is <4 Volts

Vi	Vo	Diode Status	Notes
0	4	ON	Vo=Vx; Vx=4
2	4	ON	Vo=Vx; Vx=4
4	**4**	**OFF**	**Vo=Vi; Vi=4**
5	**5**	**OFF**	**Vo=Vi; Vi=5**
10	10	OFF	Vo=Vi; Vi=10
16	16	OFF	Vo=Vi; Vi=16

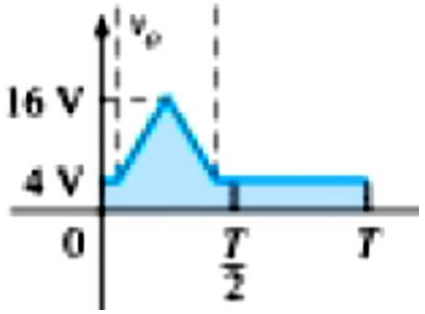
During the **Negative period**:

Forward **(ON)**	**R**everse **(OFF)**
4 Volts	
Vi	



The diode is always ON and Vo=Vx

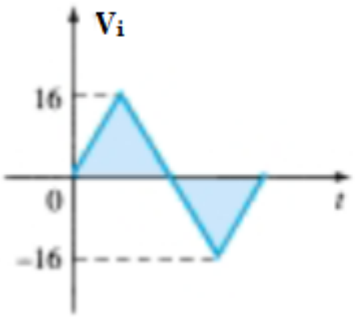
Vi	Vo	Diode Status	Notes
-1	4	ON	Vo=Vx; Vx=4
-2	4	ON	Vo=Vx; Vx=4
-4	4	ON	Vo=Vx; Vx=4
-5	4	ON	Vo=Vx; Vx=4
-10	4	ON	Vo=Vx; Vx=4
-16	4	ON	Vo=Vx; Vx=4

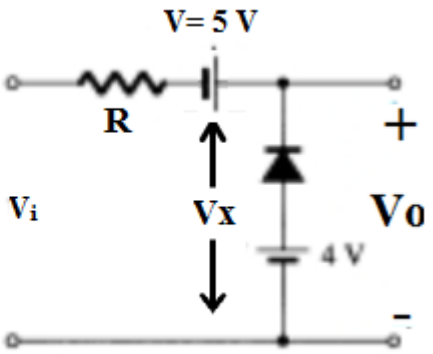


HW: Try the same examples of the series clippers using parallel configuration.

ملاحظة عامة: لفحص حالة الدايود هل هو ON او OFF

ناخذ المثال التالي:

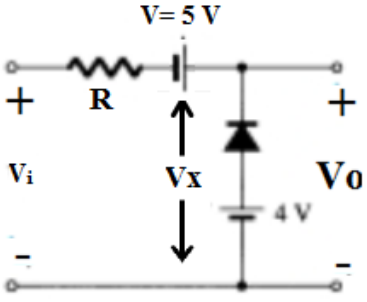




- **في هذه الدائرة ثلاثة مصادر للفولتية:**
- **5 V, 4 V and Vi**

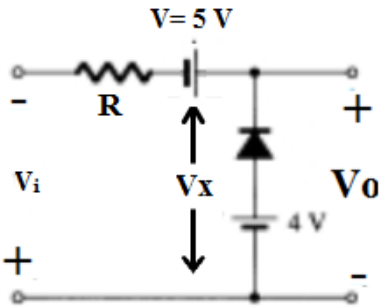
بالجزء الموجب لموجة ال Vi نرسم الدائرة بالشكل التالي:

Forward **(ON)**	**R**everse **(OFF)**
	5 Volts
	Vi
4 V	



يعني الدايود هنا دائما OFF لان الفولتية العكسية دائما اكبر من الامامية

بالجزء السالب لموجة ال Vi نرسم الدائرة بالشكل التالي:



Forward **(ON)**	**R**everse **(OFF)**
	5 Volts
Vi	
4 V	

في هذه الحالة يكون الدايود ON عندما تكون فولتية الادخال مع ال 4 فولت اكبر من ال 5 فولت .. يعني عندما تكون ال Vi>1

2.3.2 Summary

A variety of series and parallel clippers with the resulting output for the sinusoidal input are provided in the following figure.

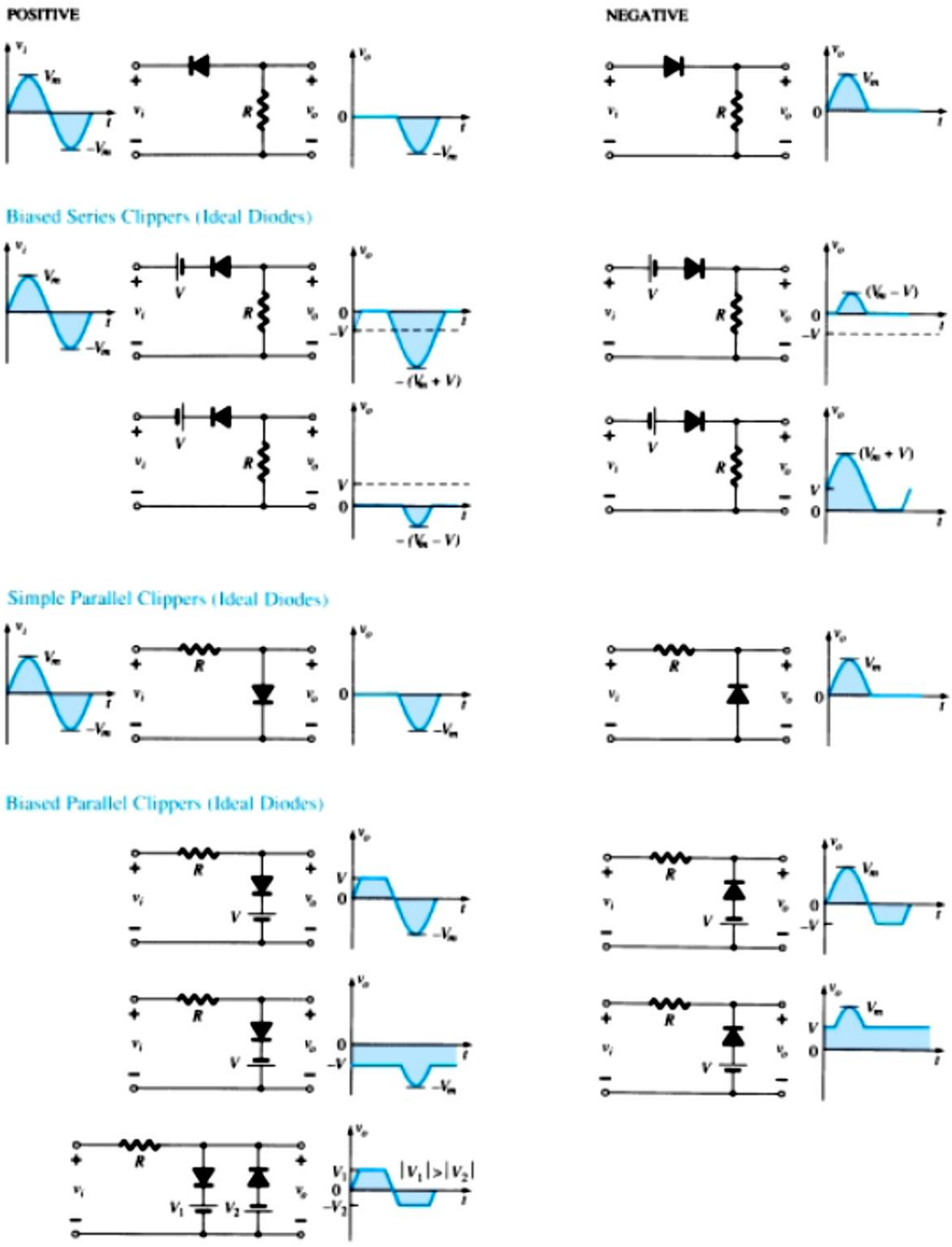


Figure : Clipping circuits.

2.4 Clampers

The *clamping* circuit is one that will "clamp" a signal to a different dc level.

The circuit must have:

- **Capacitor**
- **Diode,**
- **Resistive element**
- It can also employ an independent dc supply to introduce an additional shift.
- The magnitude of *R* and *C* must be chosen such that the time constant $\tau = RC$ is large enough to ensure that the voltage across the capacitor does not discharge significantly during the interval the diode is non-conducting.
- Throughout the analysis we will assume that for all practical purposes the capacitor will fully charge or discharge in **five time constants**.
- The network of Figure 2.25 will clamp the input signal to the zero level (for ideal diodes).

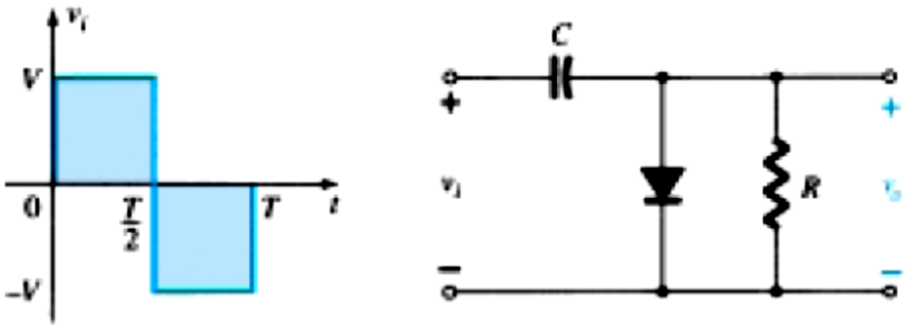


Figure 2.25: Clamper.

- Time Constant; $\tau = RC$;

  Discharging time constant $= = R \times C$

  Charging time Constant $= = R_d \times C$***; Rd is the diode forward resistance; if ideal diode Rd=0***

- **RC >> 5T/2 ; Essential condition for Clamper circuit normal operation**

In general, the following steps may be helpful when analysing clamping networks:

1. Start the analysis of clamping networks by considering that part of the input signal that will forward bias the diode.
2. During the period that the diode is in the "on" state, assume that the capacitor will charge up instantaneously to a voltage level determined by the network.

3. Assume that during the period when the diode is in the "off" state the capacitor will hold on to its established voltage level.
4. Throughout the analysis maintain a continual awareness of the location and reference polarity for vo to ensure that the proper levels for vo are obtained.
5. Keep in mind the general rule that the total swing of the total output must match the swing of the input signal.

Example 1: Determine v_o for the network of Figure 2.26 for the input indicated. And Compute the discharging time constant. And the essential condition for clamper circuit normal operation.

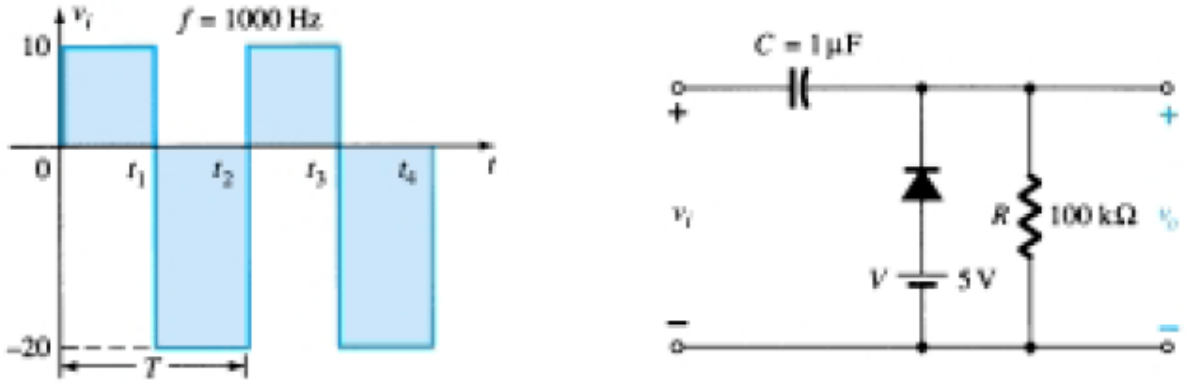
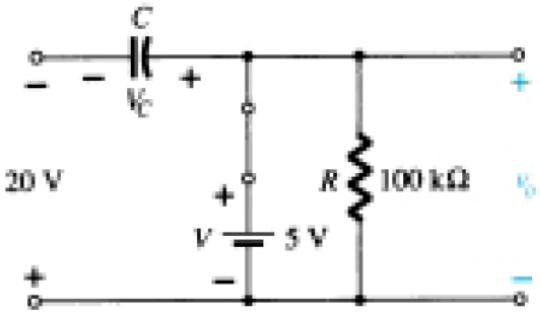


Figure 2.26: Example 1.

Solution:

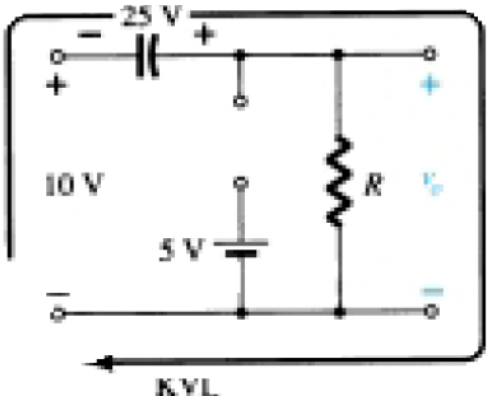
- The diode will be ON at the negative period, thus we start our analysis from the negative period **(t1 to t2 period).**



$$-20\text{ V} + V_C - 5\text{ V} = 0$$

$$V_C = 25\text{ V}$$

- The diode will be **OFF** at the positive period, **t2 to t3 period** and the circuit will look like the figure below:



$$+10\text{ V} + 25\text{ V} - v_o = 0$$

$$v_o = 35\text{ V}$$

- The time constant of the discharging network of Figure 2.26 is determined by the product *RC* and has the magnitude

1. $\tau = RC$ = (100 k)(0.1 μF) = 0.01 s = 10 ms (discharging time constant)
2. The essential condition for normal operation of total discharge time is therefore RC>> 5T/2.

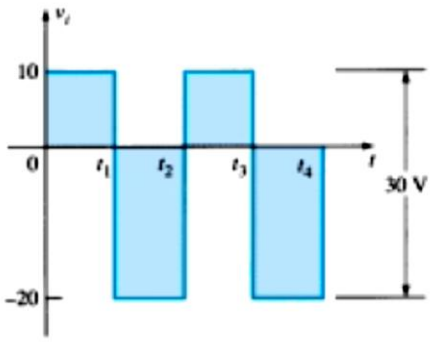
$$f = 1000\ Hz;$$

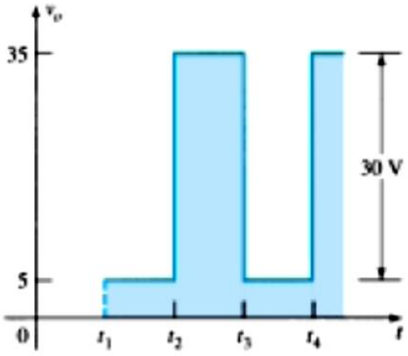
$$T = \frac{1}{f}, T = \frac{1}{1000} = 1\ m\ sec$$

$$then\ \frac{5T}{2} = \frac{5 \times 1m\ sec}{2} = 2.5\ m\ sec$$

RC=10 m sec,

As RC>> 5T/2 (10 msec>> 2.5 m sec)so the essential condition is satisfied

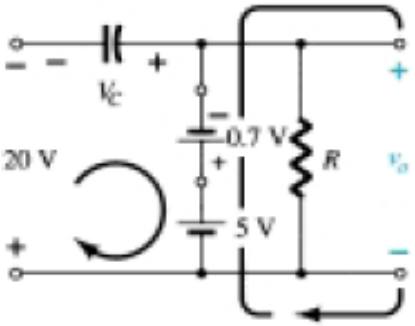




Example 2: Repeat Example 1 using a silicon diode with *VT* =0.7 V.

Solution:

- During the negative period, the diode is ON, Apply KVL on the input and output loops, as shown in the figure below:



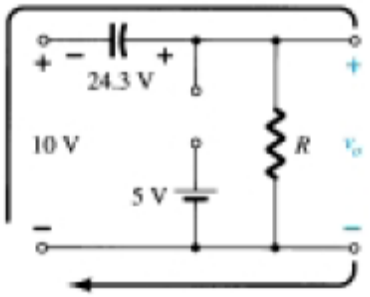
Output loop:

$$+5\text{ V} - 0.7\text{ V} - v_o = 0$$
$$v_o = 5\text{ V} - 0.7\text{ V} = 4.3\text{ V}$$

Input loop:

$$-20\text{ V} + V_C + 0.7\text{ V} - 5\text{ V} = 0$$
$$V_C = 25\text{ V} - 0.7\text{ V} = 24.3\text{ V}$$

- During the positive period (t2-t3), the circuit can be illustrated as shown below:

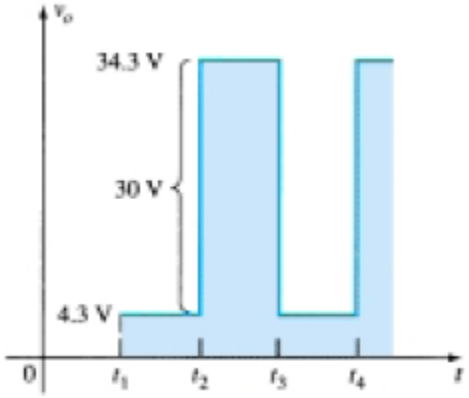


To compute v_o, apply KVL on the indicated loop:

$$+10\text{ V} + 24.3\text{ V} - v_o = 0$$

$$v_o = 34.3\text{ V}$$

Thus, the output waveform will be:



HW:

Compute Charging and Discharging Time Constant

Compute the essential condition for clamper circuits' normal operation if T=0.5 m Sec.

Summary:

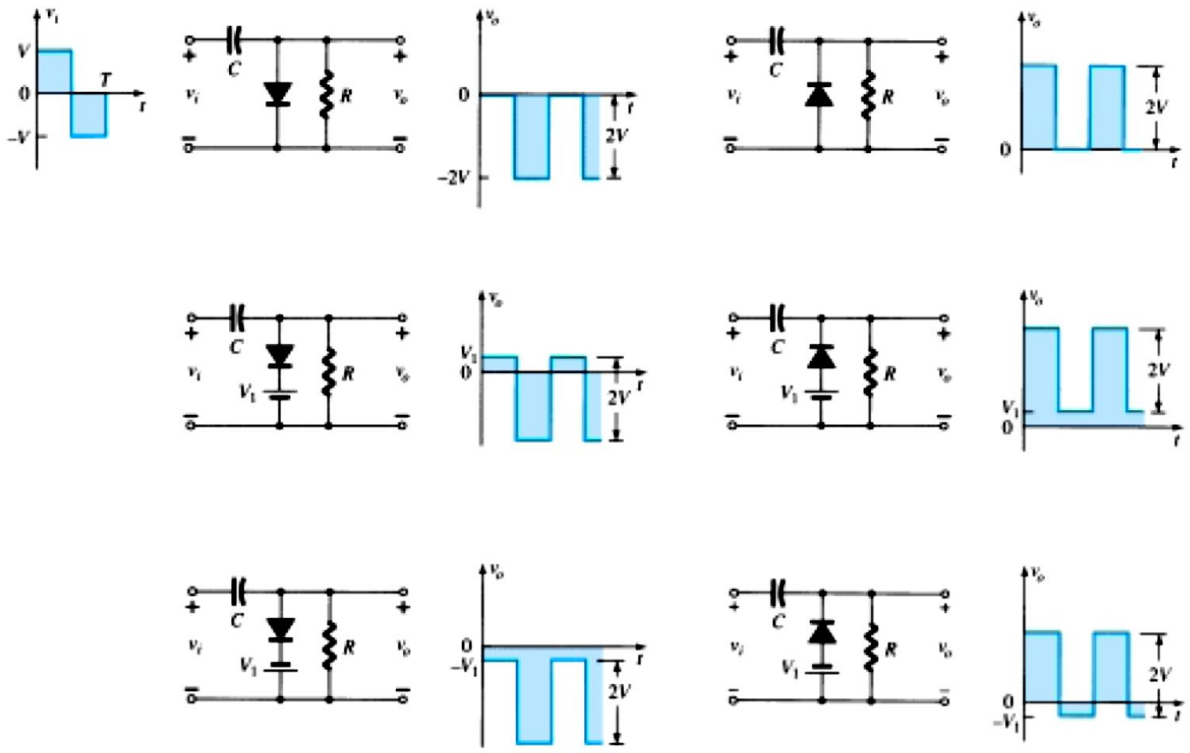


Figure 2.27: Clamping circuits with ideal diodes ($5\tau = 5RC >> T/2$).

HW: Verify the output waveform of the circuit shown below:

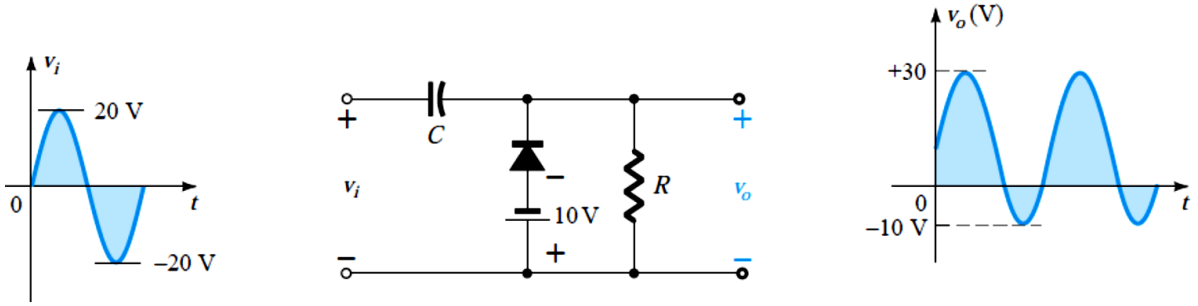


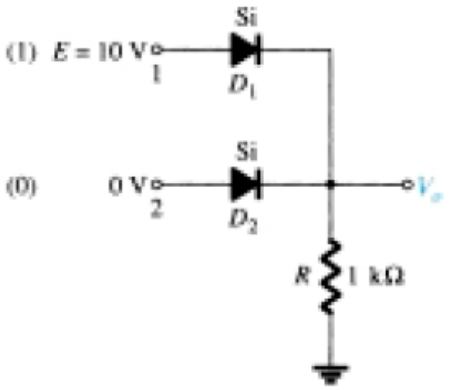
Figure 2.28: Clamping network with a sinusoidal input.

2.5 AND/OR Logic Gates

In this section we will discuss the construction and operation of AND/OR gates using Diodes:

OR-Gate:

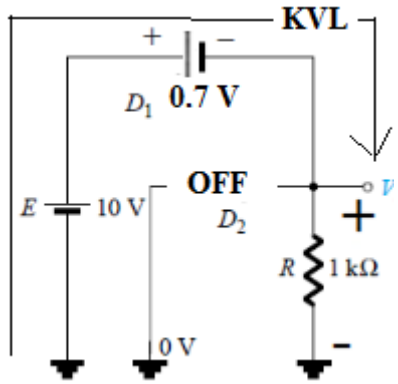
Example: Determine Vo for the network of the following Figure.



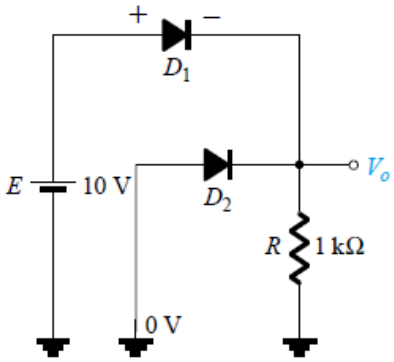
Solution:

It is OR-Gate: 1 OR 0 = 1

Logic 1 here is 10 Volts.



Redraw the circuit as shown in the following figure:



In this figure:

- 10 Volts are applied on D1, this make D1 ON-State.
- Zero Volt is applied to D2, This make D2-OFF State.
- Thus, the circuit can be redrawn as:
- Apply KVL as shown in the figure to compute Vo

  E - 0.7 - Vo=0

  10 – 0.7 – Vo=0

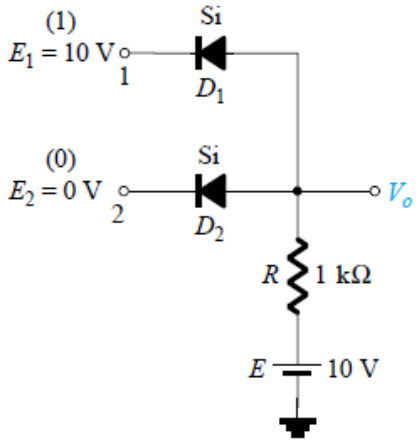
  Vo= 9.3 Volts

  We can compute the Current through R as follows:

  I=V/R= 9.3/1K= 9.3 m A

AND-Gate:

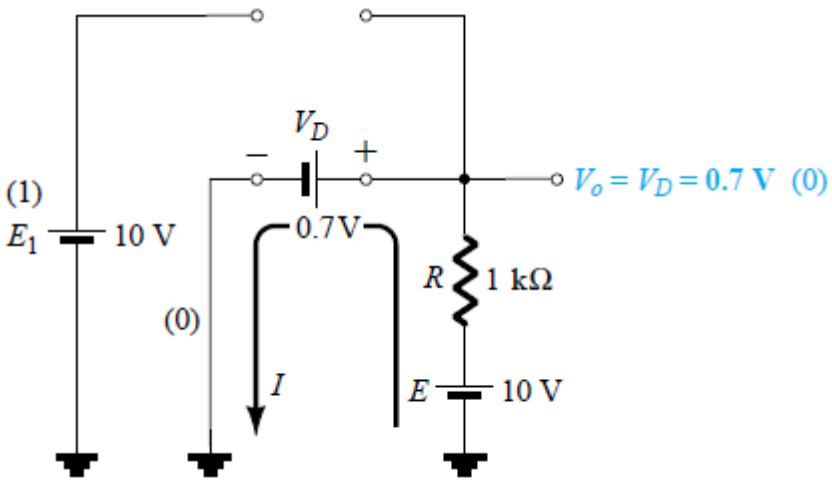
Example: Determine Vo for the network of the following Figure.



Solution:

As shown in this figure,

- **Reverse Voltage (E1=10V) on D1 is applied, so D1 is OFF.**
- **Forward Voltage (E=10V) on D2 is applied, so D2 is ON.**
- **Redraw the circuit as shown below:**



- **Apply KVL**

  0.7 – Vo = 0

  Vo=0.7 Volts

- **Can you compute the current through R????**

Notes: in logic gate if:

- **voltage <1 it can be considered as Logic Zero.**
- **Voltage>4 it can be considered as logic one.**

2.6 Power Supply

A block diagram containing the parts of a typical power supply and the voltage at various points in the unit is shown in Figure 2.28.

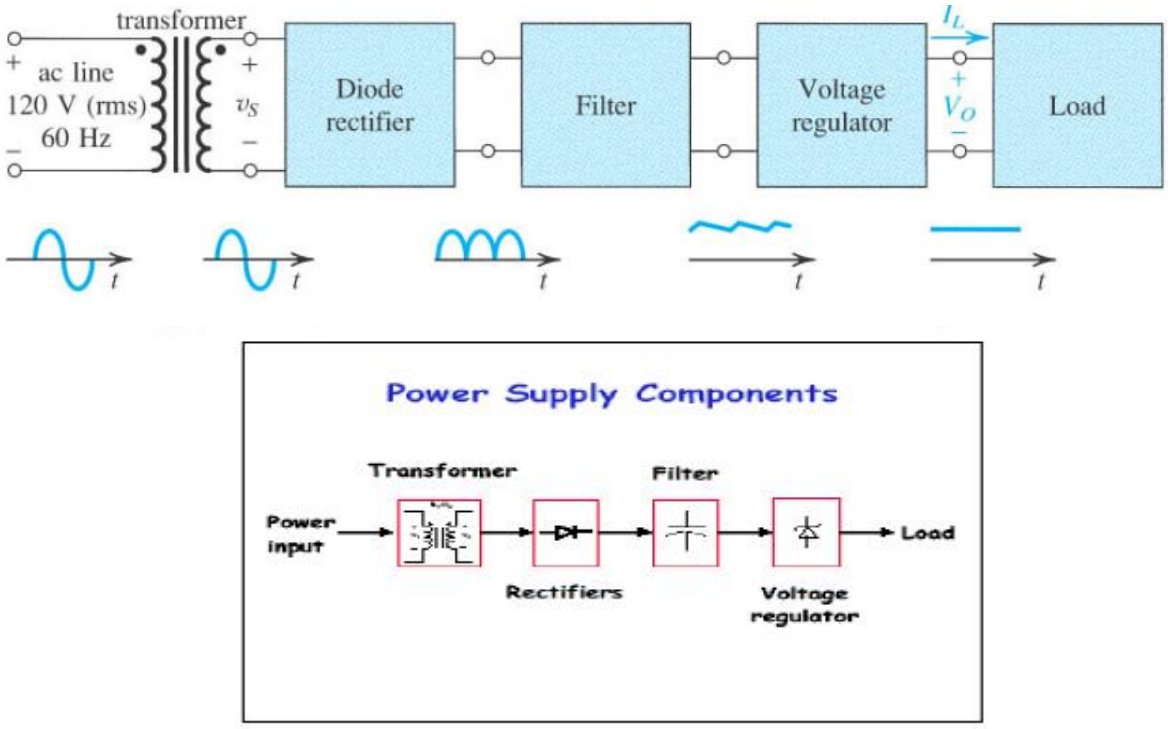


Figure 2.28: Typical Power supply configuration.

2.7 Capacitor Filter

Figure 2.29 a shows the output voltage of a full-wave rectifier before the signal is filtered, while Figureb shows the resulting waveform after the filter capacitor is connected at the rectifier output. Notice that the filtered waveform is essentially a dc voltage with some ripple (or ac variation)

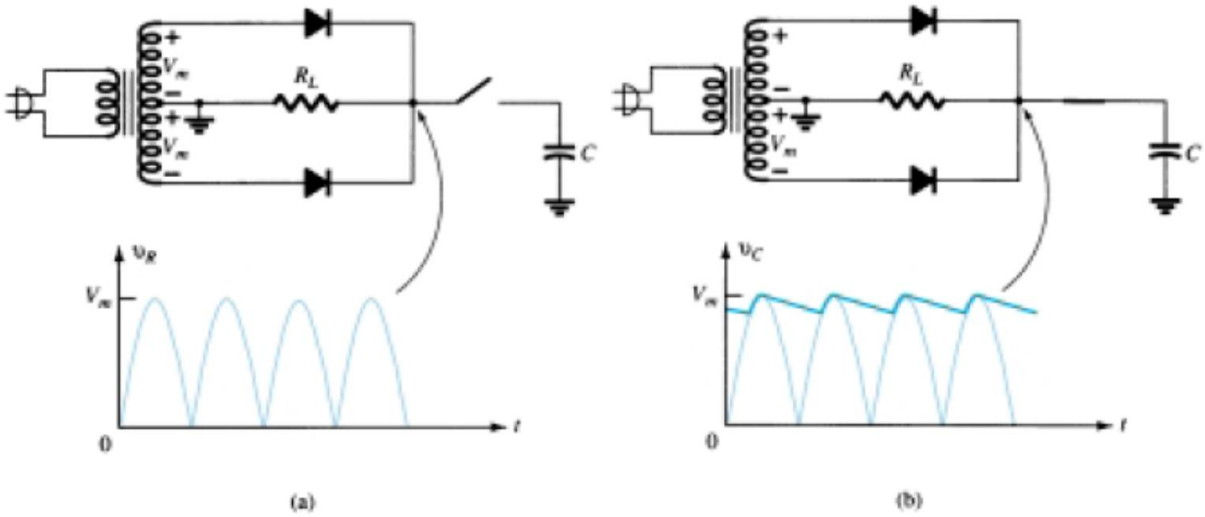


Figure 2.29: Full Wave rectifier with and without capacitor filter.

Figure 2.30 b shows the waveform across a capacitor filter with the following parameter:

- Time $\boldsymbol{t_1}$ is the charging time, diodes are ON. Charging the capacitor up to the peak rectifier voltage, $\boldsymbol{V_m}$. Time $\boldsymbol{t_2}$ is the discharging time; the diodes are OFF, the capacitor discharges through the load.
- $\boldsymbol{T/2}$ is the period of the rectified waveform; one-half the input signal frequency.
- $\boldsymbol{V_{dc}}$ is the output waveform dc level., $\boldsymbol{V_r(rms)}$ **is the** ripple voltage as the capacitor charges and discharges..

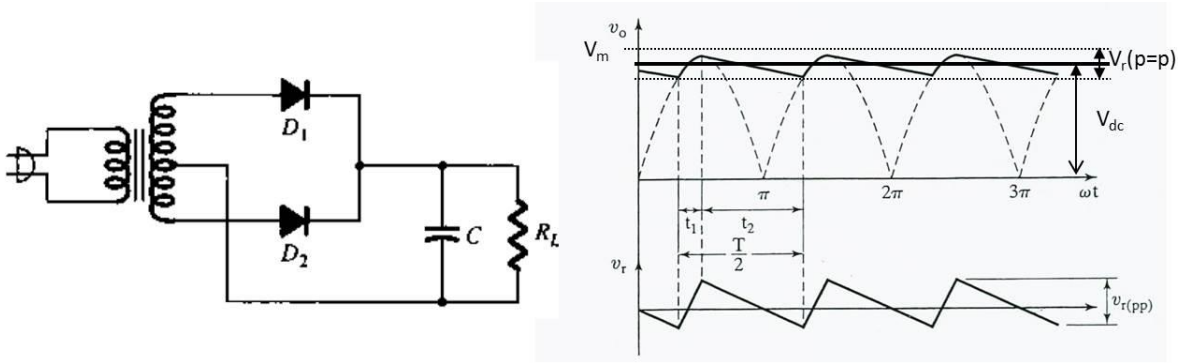


Figure 2.30: Capacitor filter: (a) capacitor filter circuit; (b) output voltage waveform..